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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,692	09/29/2003	Kyle K. Kirby	2269-5665US (02-1291.00/U	4168

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EXAMINER	
ESTRADA, MICHELLE	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 03/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,692	KIRBY, KYLE K.	
	Examiner	Art Unit	
	Michelle Estrada	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6,8-12,14-16,18,20-23 and 25-28* is/are rejected.

7)☒ Claim(s) *3,7,13,17,19 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-6, 11, 12, 14-16, 22-23 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wood et al. (6,773,938) in view of Patterson et al. (6,313,434).

Re claim 1, Wood et al. disclose providing a semiconductor substrate (200); ablating one or more depressions (210) in a surface of the semiconductor substrate to define the at least one electrical pathway extending along the surface (See fig. 5); depositing an electrically conductive material (220) over the surface of the semiconductor substrate and into the one or more depressions (Fig. 7); and planarizing the electrically conductive material at least to the surface of the semiconductor substrate to laterally isolate the electrically conductive material in the one or more depressions (Fig. 8).

Wood et al. do not specifically disclose that the depressions extend along the surface.

Patterson et al. discloses ablating a substrate along the surface (Col. 5, lines 10-16).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Wood et al. and Patterson et al. to enable the depression formation step of Wood et al. to be performed according to the teachings of Patterson et al. because one of ordinary skill in the art would have been motivated to look to alternative suitable methods of performing the disclosed depression formation step of Wood et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. See MPEP 2144.07. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Re claim 4, Wood et al. disclose wherein providing the semiconductor substrate comprises providing a silicon wafer (200) (Col. 3, lines 58-62).

Re claim 5, Wood et al. disclose wherein depositing the electrically conductive material (220) over the surface of the semiconductor substrate comprises depositing a metal (Col. 5, lines 25-30).

Re claim 6, Wood et al. disclose wherein depositing the at least on of the metal over the surface of the semiconductor substrate comprises depositing a metal selected from the group consisting of aluminum, nickel, copper, gold and alloys therof over the semiconductor substrate.

Re claim 11, Wood et al. in view of Patterson et al. as explained above, disclose providing a semiconductor substrate (200); and substantially simultaneously ablating one depression (210) in a surface of the semiconductor substrate to define the at least one conductive element in the form of an elongated trace, the at least one depression extending along the surface of the semiconductor substrate, and ablating at least one conductive structure precursor in the semiconductor substrate comprising a via (210) extending into the semiconductor substrate transverse to the surface to define the at least one conductive structure (See fig. 2d).

Re claim 12, Wood et al. disclose depositing an electrically conductive material (220) over the surface of the semiconductor substrate and into the at least one depression and the at least another depression; and planarizing the electrically conductive material at least to the surface of the semiconductor substrate to laterally

isolate the electrically conductive material in the at least one depression and the at least another depression.

Re claim 14, Wood et al. disclose wherein providing the semiconductor substrate comprises providing a silicon wafer (200) (Col. 3, lines 58-62).

Re claim 15, Wood et al. disclose wherein depositing the electrically conductive material (220) over the surface of the semiconductor substrate comprises depositing a metal (Col. 5, lines 25-30).

Re claim 16, Wood et al. disclose wherein depositing the at least on of the metal over the surface of the semiconductor substrate comprises depositing a metal selected from the group consisting of aluminum, nickel, copper, gold and alloys thereof over the semiconductor substrate.

Re claim 22, Wood et al. disclose providing a semiconductor substrate (200) having an active surface, a backside surface, and at least one sidewall oriented substantially perpendicular to the active surface and the backside surface; and ablating one or more depressions (210) in a surface of a sidewall of the semiconductor substrate to define the at least one electrical connection.

Re claim 23, Wood et al. disclose depositing an electrically conductive material (220) over the surface of the semiconductor substrate and into the one or more depressions; and planarizing the electrically conductive material at least to the surface of the semiconductor substrate to laterally isolate the electrically conductive material in the one or more depressions.

Re claim 28, Patterson et al. disclose providing a laser configured to emit a laser beam; and traversing the surface of the semiconductor substrate with the laser beam.

Claims 8, 9, 10, 18, 20, 21, 25, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wood et al. in view of Patterson et al. as applied to claims 1, 4-6, 11, 12, 14-16, 22-23 and 28 above, and further in view of Wenham et al. (6,429,037).

The combination of Wood et al. and Patterosn et al. does not disclose wherein providing the semiconductor substrate comprises providing the semiconductor substrate and forming a film over at least a portion of the surface of the semiconductor substrate, and wherein ablating one or more depressions in the surface of the semiconductor substrate comprises ablating the one or more depressions at least partially through the film.

Re claims 8, 9, 18, 20, 25 and 26, Wenham et al. disclose ablating one or more depressions in a surface of the semiconductor substrate (11) to define an electrical pathway; wherein providing the semiconductor substrate comprises providing the semiconductor substrate and forming a film (12) over at least a portion of the surface of the semiconductor substrate, and wherein ablating one or more depressions in the surface of the semiconductor substrate comprises ablating the one or more depressions at least partially through the film (Col. 4, lines 20-35).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Wood et al., Patterson et al. and Wenham et al. to enable the film formation step of of Wenham et al. to be performed in the process of the combination of

Wood et al. and Patterons et al. because the film can be used as a mask for patterning where the contact is to be formed (Col. 4, lines 20-23).

Re claims 9, 20 and 26, Wenham et al. disclose depositing an electrically conductive material (19) over the surface of the semiconductor substrate and into the one or more depressions; and Wood et al. disclose planarizing the electrically conductive material at least to the surface of the semiconductor substrate to laterally isolate the electrically conductive material in the one or more depressions.

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Wood et al. and Wenham et al. to enable the planarizing step of Wood et al. to be performed in the process of Wenham et al. because it will remove the excess metal leaving the depressions filled with inlaid metal forming the wiring.

Re claims 10, 21 and 27, Wood et al. disclose further comprising etching the one or more depressions in the surface of the semiconductor substrate subsequent to ablating and prior to depositing the electrically conductive material over the surface of the film.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wood et al. in view of Patterson et al. as applied to claims 1, 4-6, 11, 12, 14-16, 22-23 and 28 above, and further in view of Sinha (2005/0064707).

The combination of Wood et al. and Patterson et al. does not disclose wherein depositing the at least one of the metal, the conductive polymer and the conductive

nano-particles over the surface of the semiconductor substrate comprises depositing a conductive polymer selected from the group consisting of metal filled silicon and an isotropically conductive or conductor-filled epoxy over the surface of the semiconductor substrate.

Sinha discloses ablating one or more depressions (118) in a semiconductor substrate and depositing a filler material (136) comprising a conductive polymer, metal-filled silicon, isotropically or anisotropically conductive adhesives and conductor filled epoxies (Page 5, paragraph [0044]).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Wood et al., Patterson et al. and Sinha to enable the filler material formation step of Wood et al. to be the same according to the teachings of Sinha because one of ordinary skill in the art would have been motivated to look to alternative suitable methods of performing the disclosed filler material formation step of Wood et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. See MPEP 2144.07.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wood et al., Patterson et al. and Wenham et al. as applied to claims 8, 9, 10, 18, 20, 21, 25, 26 and 27 above, and further in view of Sinha (2005/0064707).

The combination of Wood et al., Patterson et al. and Wenham et al. does not disclose wherein depositing the at least one of the metal, the conductive polymer and the conductive nano-particles over the surface of the semiconductor substrate

comprises depositing a conductive polymer selected from the group consisting of metal filled silicon and an isotropically conductive or conductor-filled epoxy over the surface of the semiconductor substrate.

Sinha discloses ablating one or more depressions (118) in a semiconductor substrate and depositing a filler material (136) comprising a conductive polymer, metal-filled silicon, isotropically or anisotropically conductive adhesives and conductor filled epoxies (Page 5, paragraph [0044]).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Wood et al., Patterson et al., Wenham et al. and Sinha to enable the filler material formation step of Wood et al. to be the same according to the teachings of Sinha because one of ordinary skill in the art would have been motivated to look to alternative suitable methods of performing the disclosed filler material formation step of Wood et al., Patterson et al. and Wenham et a. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. See MPEP 2144.07.

Allowable Subject Matter

Claims 3, 7, 13, 17, 19 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michelle Estrada whose telephone number is 571-272-1858. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2800.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michelle Estrada
Primary Examiner
Art Unit 2823

ME
March 6, 2006